L Number	Hits	Search Text	DB'	Time stamp
1	959869	TAP interface with STP interface	USPAT;	2004/02/18 10:33
-	100000	, and the second	US-PGPUB;	200 1, 02, 10 10100
			EPO; JPO;	,
			DERWENT;	
			IBM_TDB	
2	821654	TAP/STP interface\$1	USPAT;	2004/02/18 10:33
-	321034	1747511 IIICHIGOCGI	US-PGPUB;	2007/02/10 10.33
			EPO; JPO;	
			DERWENT;	
3	812532	(TAP interface with STP interface) and (TAP/STP interface\$1)	IBM_TDB USPAT;	2004/02/19 10:22
	312332	(174 micriace with 511 micriace) and (177/517 micriace\$1)	US-PGPUB;	2004/02/18 10:33
			EPO; JPO;	
			DERWENT;	
4	925	"IEEE 1149.1"	IBM_TDB	2004/02/19 10:22
"	943	11177.1	USPAT;	2004/02/18 10:33
			US-PGPUB;	
ļ į			EPO; JPO;	
			DERWENT;	
	740	//TAD interface with CTD interfaces and /TAD/CTD interfaces	IBM_TDB	2004/02/10 10 5
5	748	((· · · · · · · · · · · · · · · · · ·	USPAT;	2004/02/18 10:34
		and "IEEE 1149.1"	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	2700574		IBM_TDB	
6	3789571	integrated circuit	USPAT;	2004/02/18 10:34
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
_		(//TAD: "	IBM_TDB	
7	721	(((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:37
		and "IEEE 1149.1") and (integrated circuit)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	4600705		IBM_TDB	
8	4699725	single mode test access port\$1	USPAT;	2004/02/18 10:37
			US-PGPUB;	
	:		EPO; JPO;	
	:		DERWENT;	
			IBM_TDB	
9	3557090	dual mode test access port\$1	USPAT;	2004/02/18 10:37
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
10	721	((((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:47
		and "IEEE 1149.1") and (integrated circuit)) and ((single mode	US-PGPUB;	
		test access port\$1) with (dual mode test access port\$1))	EPO; JPO;	
		,	DERWENT;	
			IBM_TDB	
11	3673415	TAP clock circuit	USPAT;	2004/02/18 10:48
			US-PGPUB;	, , _, _ , _ , _ , _
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
12	3009849	data register\$1	USPAT;	2004/02/18 10:49
1			US-PGPUB;	-30 1, 32, 10 10. 15
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
				. 1

		T	T	
13	715	(((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 10:49
		(data register \$1)	IBM_TDB	
14	881110	instruction register	USPAT; US-PGPUB;	2004/02/18 10:49
			EPO; JPO; DERWENT;	
			IBM_TDB	
15	694	((((((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:49
•		and "IEEE 1149.1") and (integrated circuit)) and ((single mode	US-PGPUB;	
		test access port\$1) with (dual mode test access port\$1))) and	EPO; JPO;	
		(data register\$1)) and (instruction register)	DERWENT;	
16	664	/////TAD interface with CTD interface) and /TAD/CTD	IBM_TDB	2004/02/10 10-50
10	004	((((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	USPAT; US-PGPUB;	2004/02/18 10:50
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)	IBM_TDB	
17	130773	multiplexer\$1	USPAT;	2004/02/18 10:50
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
10	407	//////TAD interference (III. CTD in a Company)	IBM_TDB	
18	407	((((((((TAP interface with STP interface) and (TAP/STP	USPAT;	2004/02/18 10:51
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access	US-PGPUB;	
		port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO; DERWENT;	
		(TAP clock circuit)) and multiplexer\$1	IBM_TDB	
19	1257443	TAP controller	USPAT;	2004/02/18 10:51
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
20	350	//////TAD into for a with CTD into for a larger form	IBM_TDB	
20	358	((((((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	USPAT;	2004/02/18 10:51
	į	((single mode test access port\$1) with (dual mode test access	US-PGPUB; EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)	IBM_TDB	
21	2219415	scan test port	USPAT;	2004/02/18 10:52
	-		US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
22	357	((((((((TAP interface with STP interface) and (TAP/STP	IBM_TDB USPAT;	2004/02/18 10:55
	337	interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	2007/02/10 10:55
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
	4====	(scan test port)		
23	1704259	scan path	USPAT;	2004/02/18 10:55
			US-PGPUB;	
			EPO; JPO;	
			DERWENT; IBM_TDB	
24	354	((((((((TAP interface with STP interface) and (TAP/STP	USPAT;	2004/02/18 10:55
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
		(scan test port)) and (scan path)	<u> </u>	

25	871331	core\$1	USPAT; US-PGPUB; EPO; JPO;	2004/02/18 10:55
26	203	interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:56
27	822348	(scan test port)) and (scan path)) and core\$1 scan register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:57
28	203	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:58
29	139253	accessing and (data register with first access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
30	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
31	139247	accessing and (data register with second access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
32	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:00
33	1560115	test instruction	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
34	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01

	E44056			0004/00/40 44 04
35	544856	in-circuit emulation register	USPAT; US-PGPUB;	2004/02/18 11:01
			EPO; JPO;	
			DERWENT; IBM_TDB	
36	544857	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:01
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	200 1, 02, 20 12:01
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	DERWENT; IBM_TDB	
		(scan test port)) and (scan path)) and core\$1) and (scan register))	1011_100	
		and (accessing and (data register with first access protocol))) and		
		(accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)		
37	669813	in-circuit programming register	USPAT;	2004/02/18 11:01
		and an east programming regions.	US-PGPUB;	200 1, 02, 10 11:01
			EPO; JPO;	
			DERWENT; IBM_TDB	
38	537545	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:02
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	
		((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO; DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
		(scan test port)) and (scan path)) and core\$1) and (scan register))	_	
		and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and		
		(test instruction)) afnd (in-circuit emulation register)) and		
		(in-circuit programming register)		
39	1123557	boundary scan register	USPAT;	2004/02/18 11:02
			US-PGPUB; EPO; JPO;	
:			DERWENT;	
40	692000	hypaca vanistav	IBM_TDB	2004/02/40 44-02
40	683998	bypass register	USPAT; US-PGPUB;	2004/02/18 11:03
			EPO; JPO;	
			DERWENT;	
41	545759	(boundary scan register) and (bypass register)	IBM_TDB USPAT;	2004/02/18 11:03
. -	2 .0,05	(Souridary Starr register)	US-PGPUB;	200 1/02/10 11:05
			EPO; JPO;	
			DERWENT; IBM_TDB	
42	534086	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:05
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	
		((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO; DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
		(scan test port)) and (scan path)) and core\$1) and (scan register))	_	
		and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and		
		(test instruction)) afnd (in-circuit emulation register)) and		
		(in-circuit programming register)) and ((boundary scan register)		
43	5468563	and (bypass register)) select\$4 dual mode test access port	LICDAT	2004/02/19 11:05
15	כטנטטדנ	Selector dual filode test access port	USPAT; US-PGPUB;	2004/02/18 11:05
			EPO; JPO;	
			DERWENT;	
	<u> </u>		IBM_TDB	

44	338696	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:06
11	330090	interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and (scan test port)) and (scan path)) and core\$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/13 11:00
		(in-circuit programming register)) and ((boundary scan register)		
45	5009	and (bypass register))) and (select\$4 dual mode test access port) 714/724.ccls. or 714/725.ccls. or 714/727.ccls. or 714/733.ccls. or 714/734.ccls. or 714/30.ccls. or 714/726.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 11:08
46	2324	((((((((((((((((((((((((((((((((((((((IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09
47	107	714/729.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09
48	60	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09